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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,207	KO ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-41 and 43-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11,36-41 and 43-53* is/are allowed.

6)☒ Claim(s) *13-18,27,29,30,35 and 54-57* is/are rejected.

7)☒ Claim(s) *19, 20-26, 28 and 31-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 01/24/05. A new ground of rejection as necessitated by amendment.

Claim objection

Claim 17, lines 3-4, "the first power supply voltage, said first latch" should be –the first power supply voltage and coupled to said first latch".

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 is misdescriptive to recite "each of said register including a plurality of data latch structures". However, the drawing shows that each of the data latch is a single register (see figures 6 and 7).

Claim 14 is rejected as including the indefinites of claim 13.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Ooishi et al. (USP 6621306).

As to claim 13, Ooshi's figure 1 shows a data processing apparatus comprising: data processing logic (circuit, not shown, that generating the data signals) for perforning data processing operations; a plurality of registers (the FF circuit) coupled to the data processing logic for storing data associated with the data processing operations, each the register including a plurality of data latch structures; and each said data latch structure including a first latch (44-49 in figure 3) for latching a data signal, a second latch (65-68 in figure 3) coupled to said first latch for retaining the data signal while the first latch is inoperative (sleep mode); a save device (63, 64 and circuit, shown in figure 7, that provide signal ES) connected between the first and second latches: for transferring the data signal from the first latch to the second latch, the save device including a first transistor (63) having a gate and a current path, the first latch including a node for providing the data signal to the save device, the gate connected to the node, the save device including a second transistor (transistor 75 in figure 7) in series with said current path.

As to claim 14, it is seen as an intended use for using the modified Sani et al.'s circuit in a microprocessor, a microcontroller, or digital signal processor.

As to claims 15 and 16, it is well known that wireless communication devices, i.e. cell phone and laptop computer, have memory circuits. It is seen as an intended use for using the memory circuit of Oochi's figure 1 in wireless communication devices.

5. Claims 17, 18, 27, 29, 30 and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by Zyuban et al. (US 20030188241).

As to claim 17, Zyuban et al.'s figure 6B shows a data latch apparatus, comprising: a first latch (the most left latch) coupled to receive a first power supply voltage (Wdd) for latching a data signal (I); a second latch (latch circuit in 60) coupled to receive a second power supply voltage (ground) less than the first power supply voltage and coupled to the first latch for retaining the data signal while the first latch is inoperative; a restore device (the inverters in 60 that receive signal B and N1-N8) connected between the first and second latches, the restore device having an input for receiving a restore signal (RSTR, RSTR_B), the restore device responsive to the restore signal for transferring the data signal from the second latch to the first latch; and the restore device further for isolating the second latch from the first latch independently of the restore signal while the first latch is inoperative.

As to claim 18, figure 6B shows that the second latch has a first node (SCAN_OUT) for providing the data signal to the restore device, the restore device including a first transistor (N7) having a gate connected to the first node.

As to claim 27, figure 6B shows that the second latch has a second node (SCAN_OUT_B) for providing said data signal to the restore device, the restore device including a second transistor (N3) having a gate connected to the second node.

As to claim 29, figure 6B shows that the restore device includes a third transistor (N8) connected in series with the first transistor, the third transistor having a gate connected to the input.

As to claim 30, figure 6B shows that the restore device includes a fourth (N4) transistor connected in series with the second transistor, the fourth transistor having a gate connected to the input

As to claim 35, figure 6B shows that the second latch is for retaining the data signal while the first latch is inoperative due to removal of power therefrom.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 54-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zyuban et al. (US 20030188241) in view of Sani et al. (US 2003/0218231).

As to claims 54 and 56, Zyuban et al.'s figure 6B shows all limitations of the claim except for plurality of Zyuban et al.'s cirucit figure 6B are used in a wireless communication environment. However, Sani et al.'s teaches that mobile phone having plurality of registers (latches). Zyuban et al.'s latch circuit having low leakage currents. Therefore, it would have been obvious to one having ordinary skill in the art to use plurality of Zyuban et al.'s circuit figure 6B in mobile phone for the purpose of reducing leakage currents. The modified circuit further comprises a data process logic (circuit, not shown that generating data signals) for performing data process operations; an antenna structure for permitting communication via an air interface; wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor.

As to claims 55 and 57, it is seen as an intended use for using the plurality of Zyuban et al.'s circuit figure 6 in a microprocessor, microcontroller, or a digital signal processor.

Allowable Subject Matter

5. Claims are 1-11, 36-41 and 43-53 allowed.

Claims 19, 20-26, 28 and 31-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19, 28 and 31-34 would be allowable because the prior art fails to teach or suggest first latch includes a first plurality of transistors, each transistor of the first plurality transistor having a gate oxide, the first and/or second transistor, or the third and fourth transistors having respective gate oxides which are thicker than the gate oxides of the first plurality of transistors.

Claims 20-26 would be allowable because the prior art fails to teach or suggest that the restore device includes a second transistor having a gate connected to the first node.

Claims 1-11 are allowable because the prior art fails to teach or suggest that the first transistor has a gate oxide that is thicker than the gate oxides of the plurality of transistor.

Claims 36-40 are allowable because the prior art fails to teach or suggest that an input transistor in the restore device has a second threshold voltage that is greater than the first threshold voltage of first transistor in the latch circuit.

Claims 41 and 43-53 are allowable because the prior art fails to teach or suggest that the restore device includes a first transistor and second transistor having respective to the first node.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

February 22, 2005